

OBJECTIVE: A fulltime position in Computer Engineering.

EDUCATION

MS Computer Engineering; CSU-Sacramento; GPA:3.3/4; Expected: Summer 2011

BE Electronics and Communication; Visveswaraih Technological University -2007

Certificate in Hardware & Networking; BDPS Software limited - 2006

Certificate in Embedded System Development; Indian Service Machine Institute, AICTE approved.

Related Courses:

PCI Express System Design	Advanced Data Communication Systems	Operating System Principles
Computer Aided System Design & Verification	Advanced Timing Analysis	VLSI Circuits
Adv Operating System Principles & Design	Advanced Computer Architecture	Computer Communication Networks
Micro Computer System Design I	Hierarchical Digital Design Methodology	Wireless Communication Networks
Advanced Logic Design	Microcontroller & Applications	

SKILLS

Operating Systems: Windows-95/98, 2k, 2k3, 2k8, XP, Vista, OpenSuSE, RHEL, SLES, z/OS, MAC-10.4/10.5

Microprocessors and Controllers: 8085, 8086, 8051 programming (Assembly level and C)

Programming Languages: Verilog, System Verilog, VHDL, C/C++, HTML/CSS, Perl, Python, exposure to TCL

Software & Hardware Tools: Rational Clear Quest, Rational Clear Case, Tortoise SVN, MingW, Green Hills Probe, Message Passing Interface(MPI) tool, IOMeter, SAS Analyzer, ARCCONF, BRcli, Xilinx ISE design suite, ModelSimulator, Synopsys VCS compiler, Visual Studio 2008, Eclipse Helios, Keil, MS Office, Norton Ghost, Exposure to QTP, Simics, Synopsys Primetime, Logic Analyzer, WinDbg

Communication and Leadership

- Presented a technical seminar on JTAG - Boundary Scan Architecture; IEEE Std. 1149.1 to a group of 45 engineering students at J.S.S.A.T.E college.
- Conducted software testing procedural training to groups of new recruits at Celstream Technologies.
- Multilingual: Fluent in English/Hindi/Kannada/Tamil/Japanese
- Skilled in technical writing.

PROFESSIONAL EXPERIENCE

ESD Applications Engineer co-op

PMC- Sierra Inc, Roseville

01/11- Present

Assisting the applications team in creating reference design (ASSP) and board bring up for SAS Flash Controller, setting up lab environment to recreate and analyze customer system problems related to storage protocols.

- Responsibilities include creation and running of functional validation test plans for SAS Flash Controller; board level debug to ensure link-up, discovery.
- Assist in performance characterization for SAS Protocol Controllers, collecting firmware trace and memory dumps from host bus adapter registers; embedded firmware debug/development.
- Develop Perl scripts and modules for configuring, running and reporting tests on MaxRaid and Adaptec SAS RAID Controllers.
- Creating and burning firmware images onto controllers flash using command line tools and GHS Probe.
- Prepare customer deliverable application notes; device data sheet errata and supporting wiki pages.
- Trained in different storage protocols/products like PCIe, SCSI, SAS, SATA, Flash, SSD, RAID.

Graduate Intern

DTL Corporation, Davis

06/10-11/10

Worked in the research and development wing for Mori Seiki; debugging the interpreter module and GUI of the simulation software developed by DTL Corporation. Responsibilities included creation of automation framework for testing the simulation software using python and assisting the team in preparing for release. Performed test development from specifications; created code to test different scenarios; logged defects and crash dumps; assisted developers in resolving software defects.

Software Test Engineer

Celstream Technologies, Bangalore

06/07-07/08

Configured and debugged defects in XEROX printer and scanner device drivers using IpSecurity features in peer to peer as well as client/server environment on various operating system platforms. Worked on multi-function devices and performed test development and automation on printer management applications such as Usage Analysis Tool and Font Management Utility.

ACADEMIC PROJECTS

- Master's Project** *CSU, Sacramento* *09/10-Present*
G7.11 audio codec and SIP protocol based VoIP implementation on TLS/IPsec encryption system: My master's project involves using G7.11 codec U-law algorithm for VoIP implementation. The system uses Session Initiation Protocol (SIP) supported by TCP to transfer packetized audio over network. This SIP implementation provides high levels of security by incorporating IPsec encryption standards to ensure secure communication over network.
- Advanced Operating System Principles & Design** *CSU, Sacramento* *09/09-12/09*
Created an application to measure the performance of a remote windows server by tracking system resources like processes, CPU, memory, network and disk utilization on a real time basis. Applied knowledge about Linux internals and worked on creation and insertion of new modules for existing device drivers on Linux.
- Advanced Data Communication System** *CSU, Sacramento* *01/09-05/09*
- **Framing and Error Checking:** Implemented a data link layer on top of a virtual physical layer by building a message, transmitting and receiving data packets and verifying the correctness of each transmission and Implemented LZW scheme for message compression and decompression.
 - **Flow Control, Error Control and Piggybacking:** Implemented sliding window protocol on the message along with negative acknowledgement.
- Micro Computer System Design I** *CSU, Sacramento* *01/09-05/09*
- **PCI Card:** Designed initiator device to initiate optimized read transaction for 4 bytes from a given address. The target returned the data showing all of the appropriate cycles.
 - **Cache-Memory Subsystem Design:** Designed a cache subsystem for a Pentium-Pro processor. The processor data bus width was 256bits and the address bus was 36bits. The cache subsystem was a 4 way set associative look-through cache (L1), each 2KB in size. The cache system used write back policy and had a bus master doing read cycles.
- PCI Express System Design** *CSU, Sacramento* *01/10-05/10*
Designed and verified a PCIE system which performed posted memory writes to a specific location of another end point device. System also incorporated ACK/NAK generation mechanism for verification of transmission and reception of data packets.
- Computer Aided System Design & Verification** *CSU, Sacramento* *09/09-12/09*
Designed, verified and validated a system with an arbiter that grants DMA bus access to one of N possible clients which were configured using registers based on the specification provided. System incorporated "round-robin" policy and used constrained-based randomization to generate test vectors (varying transaction type, size, address) to validate the design under test.
- Advanced Logic Design** *CSU, Sacramento* *09/08-12/08*
- **ADC-SRAM Interface Design:** Using Verilog and Xilinx Virtex FPGA board performed read and write of data from the ADC output to the SRAM and displayed the current data on the LCD display.
 - **Flash-SRAM Interface Design:** The design read data from Flash and wrote to a specific address in SRAM using Verilog and Xilinx Virtex FPGA board.
 - **Verilog / VHDL Hardware Projects:** ALU RTL design, sequence detector design, keypad interface, calculator design, scrolling LCD display, traffic signal controller design, counter design, real time clock design, ASIC, SoC design, Moore and Mealy FSM design in Xilinx ISE.

ACHIEVEMENTS AND PROFESSIONAL AFFILIATIONS

- Received recognition from my team lead for my fine work and attention to details in finding a critical defect in a major device driver release.
- Winner, Part One, "IBM Master the Mainframe" contest.
- Achieved 100% marks in pre-university physics.
- Active member, IEEE (2007-2008) and Association for Computing Machinery (2009)
- Founding member, Student Chapter of Indian Society of Technical Education at JSSATE

References available upon request