



## ACADEMIC PROJECTS

- Advanced Operating System Principles & Design**      *CSU, Sacramento*      *09/09-12/09*
- Created an application to measure the performance of the system by tracking resources like CPU usage, memory utilization on a real time basis. Applied knowledge about the kernel internals and worked on creation and insertion of new modules for existing device drivers on Linux.
- Advanced Data Communication System**      *CSU, Sacramento*      *01/09-05/09*
- **Framing and Error Checking:** Implemented a data link layer on top of a virtual physical layer by building a message, transmitting/receiving data and verifying the correctness of transmission.
  - **Compression and Decompression:** Implemented LZW scheme on the above mentioned project.
  - **Flow Control, Error Control and Piggybacking:** Implemented sliding window protocol on the message along with negative acknowledgement.
- Computer Aided System Design & Verification**      *CSU, Sacramento*      *09/09-12/09*
- Designed, verified and validated a system with an arbiter which would grant DMA bus access to one of N possible clients which were configured using registers based on the specification provided. System incorporated round robin policy and used constrained-based randomization to generate test vectors (varying transaction type, size, address) to validate the Design under Test.
- Hierarchical Digital Design Methodology**      *CSU, Sacramento*      *01/09-05/09*
- **Parallel-to-Serial Transmit Interface** design (Using Synopsis VCS): Designed, simulated and synthesized a Parallel-to-Serial interface (PSI) capable of receiving a packet data, appending start and end delimiters to the packet, converting it to serial data, and transmitting it through a serial output. On one side, PSI was connected to a Direct Memory Access (DMA) master that would send it a packet to be transmitted. On the other side, it was connected to a Digital-to-Analog converter.
- Micro Computer System Design I**      *CSU, Sacramento*      *01/09-05/09*
- **PCI Card:** Designed initiator device to initiate optimized read transaction for 4 bytes from a given address and the target returned a specific data showing all the appropriate cycles.
  - **Cache-Memory Subsystem Design:** For Pentium-Pro processor we designed a cache subsystem with processor data bus width being 256bits and address bus 36bits. It was a 4 way set associative look-through cache in the system (L1) each 2KB in size. Cache system used write back policy & had a bus master doing read cycles.
- Advanced Logic Design**      *CSU, Sacramento*      *09/08-12/08*
- **ADC-SRAM Interface Design:** Performed read and write of data from the ADC output to the SRAM using Verilog and Xilinx Virtex FPGA board and displayed the current data on the LCD display.
  - **Flash-SRAM Interface Design:** Design read data from Flash and wrote to a specific address in SRAM using Verilog and Xilinx Virtex FPGA board.
  - **Verilog / VHDL Hardware Projects:** ALU RTL design, sequence detector design, keypad interface, calculator design, scrolling LCD display, traffic signal controller design, counter design, real time clock design, ASIC, SoC design, Moore and Mealy FSM design in Xilinx ISE.
- Advanced Computer Architecture**      *CSU, Sacramento*      *09/08-12/08*
- Created single and multi processor shared memory virtual systems using Virtutech Simics tool and simulated their performance when a multi-threaded program executes on it with different cache sub systems.
  - Learned computer classification schemes, fine and coarse grain parallelism, processor interconnections, cache coherence protocols and performance issues of multiprocessor systems.

## ACHIEVEMENTS AND PROFESSIONAL AFFILIATIONS

- Received recognition from my team lead for my fine work and attention to details in finding a critical defect in major device driver release.
- Winner, Part One, "IBM Master the Mainframe" contest.
- Achieved 100% marks in pre-university physics.
- Active member, IEEE (2007-2008) and Association for Computing Machinery (2009)
- Founding member, Student Chapter of Indian Society of Technical Education at JSSATE.